line and a write voltage on the data line to induce charge to migrate from a channel in a substrate through [a] an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

48. (Amended) The method of claim 47 wherein:

programming comprises programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce hot electron injection from a channel in a substrate through [an] the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor; and

erasing comprises applying an erase voltage of less than 12 Volts to the floating gate transistor to erase the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling.

Please add the following new claims:

51. (New) The method of claim 16 wherein reading data comprises reading data by detecting a current between a source and a drain in a silicon substrate.

52. (New) The method of claim 43 wherein programming comprises programming the floating gate transistor by inducing charge to migrate from a channel between a source and a drain in a silicon substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor.

53. (New) The method of claim 47 wherein programming comprises programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce charge to migrate from a channel between a source and a drain in a silicon substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode

in the floating gate transistor.

26
54. (New) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and an amorphous silicon carbide (a-SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV; and

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate.

27 26
55. (New) The method of claim 54, further comprising erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

28 26
56. (New) The method of claim 54, further comprising refreshing the charge placed on the floating gate electrode.

29 28
57. (New) The method of claim 56, wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals.

30 26
58. (New) The method of claim 54 wherein programming further comprises programming the floating gate electrode by inducing charge to migrate from a channel between a source region and a drain region in a silicon substrate through the amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode.

31
59. (New) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

storing data on a floating gate electrode in the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line such that charge is carried from a substrate to the floating gate electrode through an amorphous silicon carbide (a-SiC) gate